reconfiguring said system to perform comparison with memory information from other processors without using faulted processors;

sending a rendezvous signal to said first processor;

receiving a rendezvous signal from said first processor; and

updating the clock of said first processor and said second processor based on the clocking midpoint of all processor signals.

84. (Twice Amended) A method of voting between a plurality of processors having memory comprising the steps of:

exchanging information between said processors;

comparing information in selected categories in each processor, with the information received from other processors in the same selected category;

determining if said information conforms in a majority of processors in said category; and

restoring said conformed category of information in all non-conforming processors;

sending a rendezvous signal to the other processors;

receiving a rendezvous signal from the other processors; and

sending update signals to the clock based on the clocking midpoint of all processor signals.

## *REMARKS*

By the foregoing Amendment, Applicants have sought to amend claims 1, 6, 7, 11-13, 16, 21-22, 28-29, 32-35, 50-53, 69, 71, 77, and 93-94 in order to expedite prosecution of this matter. Applicants have also sought to cancel claims 17-20, 39-43, 45, 48-49, 55, 57, 63-64, 66-68, 74, 100-101, 104, 105 and 107 without prejudice or disclaimer. Upon entry of the foregoing Amendment, claims 1-16, 21-38, 44, 50-53, 69, 71, 77, and 93-98 remain pending in the present application.

Based on the above Amendment and the following Remarks Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

***Interview***

Applicants thank Examiner Baderman for conducting a telephonic Interview with Applicants' representative on February 27, 2002. During the Interview, Applicants' representative discussed subject matter set forth in claim 50. Applicant proposed an Amendment to include similar subject matter in the pending independent claims in an effort to expedite prosecution. The Examiner agreed to consider such an Amendment.

***Objection to the Specification***

The Examiner objected to the Specification as not having an Abstract. Applicants have added an Abstract as set forth in the above Amendment.

The Examiner objected to the disclosure because of an informality in the Brief Description of the Drawings with regard to Figure 18. Applicants have amended the description to accommodate the Examiner as set forth in the above Amendment.

***Restriction Requirement and Election Under 35 U.S.C. § 121***

The Examiner has restricted the claims into two separate groups, namely:

Group I, which includes claims 1-45, 48-53, 55, 57, 63-64, 66-69, 71, 74, 77, 93-98, 100-101 and 104-105; and

Group II, which includes claim 107.

For purposes of expediting prosecution of this matter, Applicants requested that the Examiner examine the claims corresponding to Group I without traverse. Claim 107 is canceled by the above amendment without prejudice or disclaimer.

***Objections to Claims 17, 22, 32, 35, 39, 43, and 50***

The Examiner objected to claims 17, 22, 32, 35, 39, 43, and 50 based on various informalities. Applicants have amended claims 22, 32, 35, and 50 to accommodate the Examiner. Applicants have canceled claims 17, 39, and 43 without prejudice or disclaimer thereby rendering these objections moot.

***Objections to Claims 48-49, 63-64, 66-68, 100, and 101***

The Examiner objected to claims 48-49, 63-64, 66-68, 100, and 101 because the claims from which these claims depend were canceled. Applicants have canceled each of these claims without prejudice or disclaimer.

***Double Patenting***

The Examiner objected to claims 39-42 and 45 as being substantially duplicative of claims 35-38 and 44. Applicants have canceled claims 39-42 and 45 without prejudice or disclaimer.

***Rejection of Claims 1-45, 51-53, 55, 57, 69, 71, 74, 77, 93-98, 104 and 105 Under 35 U.S.C. § 102(b)***

The Examiner has rejected claims 1-45, 51-53, 55, 57, 69, 71, 74, 77, 93-98, 104 and 105 as being unpatentable over U.S. Patent No. 4,967,347 to Smith *et al.* ("Smith"). Claims 17-20, 39-43, 45, 48-49, 55, 57-58, 63-64, 66-68, 74, 100, 101, 104, 105 and 107 have been canceled thereby rendering the rejection of these claims moot.

Independent claims 1, 6, 11, 16, 21, 29, 34, 51, 53, 69, 71, 77, and 93-94 have been amended to include features similar to those found in claim 50 which the Examiner indicated as including allowable subject matter. Applicants submit that these amended claims are now also allowable over Smith. The remaining pending claims depend from or add additional features to these independent claims. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejections of the pending claims.

## *Conclusion*

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that further personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Dated: 27 February 2002

Respectfully submitted,
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Enclosure: Appendix indicating Amendments to Claims

## APPENDIX

1. (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] at least one input/output module for receiving and sending control information to said control elements, communicating with each main processor module;

[c.] at least one communication module communicating external signals to said plurality of main processor modules;

[d.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[e.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of main processor modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules;

a system for determining the clocking midpoint of all processor signals;

a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint;

a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint; and

[f. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

g.] a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors[;

h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings].

6. (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] at least one input/output module for receiving and sending control information to said control elements communicating with each main processor module;

[c.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[d.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of main processor modules and compares the information in each selected main processor module with the information in other selected ones of said main processor modules;

[e.] a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules;

a system for determining the clocking midpoint of all processor signals;

a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint

[f. a channel transmission validity testing system;

g. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings].

7. (Twice Amended) A controller as described in claim 6 wherein there are a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors and wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, and other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module.

11. (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] at least one input/output module for receiving and sending control information to control elements, communicating with each main processor module;

[c.] at least one communication module communicating external signals to said plurality of main processor modules;

[d.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[e.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

[f.] a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules;

a system for determining the clocking midpoint of all processor signals;

a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint

[g. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical receptacles to each of said housings].

12. (Twice Amended) A controller as described in claim 11 wherein there are a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors and wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

13. (Twice Amended) A controller as described in claim 11 wherein there are a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors and wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

16. (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

[c.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[d.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals

[e. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

f. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

g. at least one base plate circuit board for mounting each module which provides base plate electrical receptacles for receiving the housing electrical connectors; and

h. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings].

21. (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[c.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

[d.] a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

[e.] a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

[f.] at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals

[g. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings].

22. (Twice Amended) A controller as described in claim 21 wherein there are a plurality of base plate circuit boards[, selected ones of said base plate circuit boards] receiving said housing for said main processor modules[, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module].

28. (Twice Amended) A controller as described in claim 21 further comprising:

[a.] at least one input/output module for receiving and sending control information to control elements in said control system communicating with each of said plurality of main processor modules; and

[b.] at least one communication module for sending and receiving external signals communicating with each of said plurality of main processor modules.

29. (Twice Amended) A control system platform for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

[c.] at least one communication module communicating external signals to said plurality of main processor modules;

[d.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[e.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

[f.] a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

[g.] a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals

[h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings].

32. (Twice Amended) A control system platform as described in claim 31 [29] wherein said fastener is an elongated screw which is rotatable attached to said housing along its

length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

33. (Twice Amended) A control system platform as described in claim 31 [29] further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

34. (Twice Amended) A control system platform for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

[c.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[d.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

[e.] a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

[f.] a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

[g.] at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; [and

h.] a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

35. (Twice Amended) A control system platform as described in claim 34 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, and other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module[, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module].

50. (Twice Amended) A computer control system for executing an application program to process control information related to control elements comprising:

[a.] a plurality of main processor modules each of which runs the application program;

[b.] at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

[c.] a time synchronizing system for synchronizing the time clocks of said main processor modules;

[d.] a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

[e.] a selection system which determines which of said plurality of main processor modules is a selected main processor module which is used to compare information in each main processor module;

[f.] a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards;

[g.] a common rail system for mounting of said housings and providing electronic connections to each of said housings;

[h.] apparatus for sending a rendezvous signal to all other main processor modules;

[i.] apparatus for receiving a rendezvous signal from [form] all other main processor modules;

[j.] a system for determining the clocking midpoint of all processor signals;

[k.] a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

[l.] a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint.

51. (Twice Amended) A control system platform for executing a control system program for managing a control system and evaluating the accuracy of information related to said control system, said platform comprising:

[a.] a plurality of main processor modules, each executing a copy of said application program;

[b.] at least one field input/output module communicating with each main processor module;

[c.] a voting system for comparing information between said main processor modules;

[and

d.] a restoring system for restoring valid information for access by said main processor modules;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

52. (Twice Amended) A control system platform as described in claim 51 wherein said information is selected from the group consisting of:

[a.] program code,

[b.] fault detection information,

[c.] sensor information,

[d.] command information,

[e.] output information, and

[f.] input information[, and

g. any combination of a through f].

53. (Twice Amended) A control system for executing an application program and evaluating the accuracy of input/output information comprising:

[a.] a plurality of main processor modules, each executing said application program;

[b.] at least one field input/output module communicating with each main processor module; [and

c.] a voting system for comparing information between said main processor modules; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including:

apparatus for sending a rendezvous signal to all other main processor modules,

apparatus for receiving a rendezvous signal from all other main processor modules, and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

69. (Twice Amended) A voting system which exchanges information between selected ones of a main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules comprising:

[a.] an apparatus for loading control system related information from each processor for storage in every other processor;

[b.] a comparison apparatus for comparing loaded control system related information with the comparing processor's control system information;

[c.] memory for storing the results of said comparison;

[d.] a selection apparatus for determining which loaded information compares with said comparing processor's information; [and

e.] a default apparatus for storing a default indication where the comparing processor's information fails to compare with a majority of said loaded processor information; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including:

apparatus for sending a rendezvous signal to all other main processor modules,

apparatus for receiving a rendezvous signal from all other main processor modules, and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

71. (Twice Amended) A control system for executing an application program and evaluating the accuracy of input/output information comprising:

[a.] a plurality of main processor modules;

[b.] at least one field input/output module communicating with each main processor module; [and

c.] a voting system for comparing information between said main processor modules; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including:

apparatus for sending and receiving rendezvous signals to and from all other main processor modules, and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

77. (Twice Amended) A control system platform for running a control system program which processes information related to a control system; said control system platform comprising:

[a.] a plurality of processors executing said control system program and processing said control system information said processors mounted to a common power rail;

[b.] at least one input/output module for sending and receiving said information related to said control system; communicating with each of said processors mounted to said common power rail communicating with said plurality of processors;

[c.] at least one communication module for receiving external signals and exchanging external signals with each of said processors and external signals; mounted to said common power rail communicating with said plurality of processors over a communications bus;

[d.] a validation system on each processor for evaluating said control system information to be processed by said control system program prior to processing by said control system program; said evaluation system comparing categories of information stored in memory on each processor with the same category of information in memory on other processors and selecting information on which a majority of processors compare as valid information and storing said valid information into the memory of any processor for which the information did not compare with the majority of processors;

[e.] each of said processors being interconnected on an inter-processor bus through a loop-back path; said loop back path applying the signals for transmitting information by each transmitting processor to other processors on said bus as an attenuated loop-back signal to said transmitting processor;

[f.] a storage area in the transmitting processor memory for storing said loop-back information; [and

g.] a comparator for comparing signals transmitted by said other processors on said bus with said loop back signals to determine if the information in said loop-back signals is the same as the signals transmitted by said other processors; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including apparatus for sending and receiving rendezvous signals to and from all other main processor modules and a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

93. (Twice Amended) A method for determining the voting mode of a plurality of processors each having memory and coupled to a inter processor bus comprising the steps of:

[a.] exchanging information with said plurality of processors over said bus transmitting a category of information from a first processor on said bus to a second processor on the bus;

[b.] passing said transmitted information through an attenuated loop-back path to said first processor;

[c.] capturing said transmitted loop-back information in said first processor memory;

[d.] comparing said attenuated loop back information captured in said first processor memory with the information transmitted by said first processor;

[e.] storing a first result of said comparing in said first processor's memory;

[f.] faulting the first processor when the first result indicates a difference in said information;

[g.] capturing second processor information which is received by said first processor from a second processor on said bus in said first processor memory;

[h.] comparing said second processor captured information with the same category of information in said first processor;

[i.] faulting the second processor when the second result indicates a difference in said information; [and

j.] reconfiguring said system to perform comparison with memory information from other processors without using faulted processors;

sending a rendezvous signal to said first processor;

receiving a rendezvous signal from said first processor; and

updating the clock of said first processor and said second processor based on the clocking midpoint of all processor signals.

94. (Twice Amended) A method of voting between a plurality of processors having memory comprising the steps of:

[a.] exchanging information between said processors;

[b.] comparing information in selected categories in each processor, with the information received from other processors in the same selected category;

[c.] determining if said information conforms in a majority of processors in said category; [and

d.] restoring said conformed category of information in all non-conforming processors;

sending a rendezvous signal to the other processors;

receiving a rendezvous signal from the other processors; and

sending update signals to the clock based on the clocking midpoint of all processor signals.